IN THE SPECIFICATION:

Paragraph [0003] has been amended as follows:

In order to meet demands for higher density, semiconductor packages in recent years include wiring patterns which are disposed ~~closely~~ close to one another. Accordingly, such semiconductor packages would incur problems such as an occurrence of crosstalk noises between a plurality of wiring, or fluctuation of electric potential of power source line and the like. In particular, a package for mounting a semiconductor element for high-frequency use, in which high-speed switching operations are required, tends to incur crosstalk noises along with an increase in frequency or incur switching noises because a switching element therein is turned on and off in a high speed. As a result, electric potential of a power source line and the like tends to vary easily.

Paragraph [0024] has been amended as follows:

The semiconductor package 10 of this embodiment is basically characterized by the built-in capacitor portions, more specifically, by formation of the resin layers 13a, 13b and 13c by the electrophoretic deposition process (to be described later) on the wiring layers 12a, 12b and 12 formed on [[the]] both surfaces of the insulative base members 11a, 11b and 11c used as the core members of the printed wiring boards, and further by use of the respective resin layers as dielectric layers of the capacitor portions.

Paragraph [0025] has been amended as follows:

The semiconductor package 10 of this embodiment is also characterized by the multilayer wiring structure thereof, which is formed by laminating that the predetermined number of the printed wiring boards provided with the capacitor portions to form the laminated core portion 10a, and by laminating the predetermined number of the layers (which are two layers in the illustrated example) on [[the]] both surfaces of the laminated core portion 10a in accordance with the build-up method to form the build-up wiring portions 10b.

Paragraph [0026] has been amended as follows:

The respective resin layers 13a, 13b and 13c constitute the dielectric layers of the respective capacitor portions. Accordingly, in terms of characteristics of the capacitors, it is preferable that the respective resin layers 13a, 13b and 13c are made of materials having a high dielectric constant. In this embodiment, the resin layers 13a, 13b and 13c are made of polyimide resin blended with inorganic filler having high dielectric constant (wherein the dielectric constant thereof is 20 or higher, for example). Moreover, each of the pins 26 electrically connected to the respective wiring layers 12a, 12b and 12c through the conductors 16, the respective wiring layers 17 and 20, the conductors 23 and the plated films 25, constitutes a first electrode of each of the capacitor portions. Meanwhile, each of the pins 26 electrically connected to the respective wiring layers 14a, 14b and 14c formed on the respective resin layers 13a, 13b and 13c through the conductors 16, the respective wiring layers 17 and 20, the conductors 23 and the plated films

25, constitutes a second electrode of each of the capacitor portions.

Paragraph [0036] has been amended as follows:

The wiring layers 14a can be formed by a ~~similar~~ process similar to the process performed in the step of FIG. 2A. Specifically, photosensitive dry films are attached to surfaces of the conductive layers (the Cu layers) formed on the insulative base member 11a and the resin layers 13a. Then, the dry films are subjected to exposure and development in accordance with predetermined shapes using masks (patterning the dry films), whereby openings are formed on the dry films at the portions other than the portions corresponding to the predetermined shapes. Thereafter, the copper layers at the portions corresponding to regions of the openings are removed by wet etching, for example. Finally, the dry films are peeled off. In this way, it is possible to form the wiring patterns (the wiring layers 14a) of the predetermined shapes. Each of the wiring layers 14a thus formed constitutes a second electrode layer of each of the capacitor portions.